# INTEGRATED CONTINUOUS-TIME

# FILTERS

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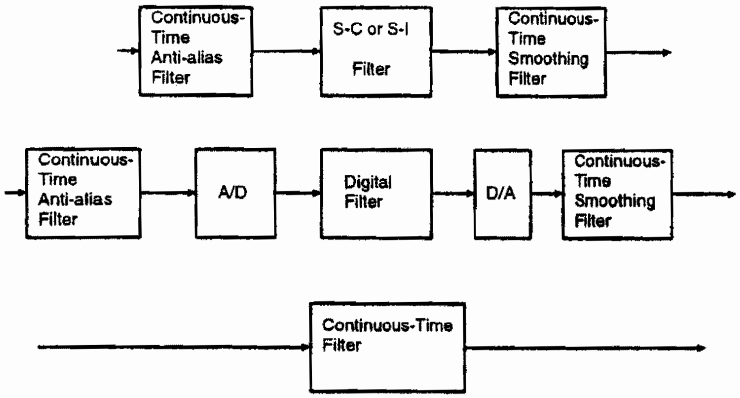
## OVERVIEW

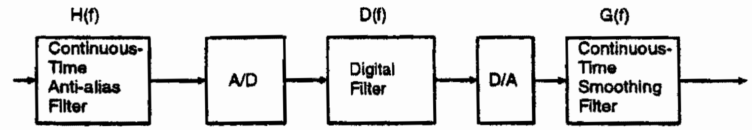
- Overview of applications for continuous-time filters
- State-variable synthesis techniques
- Gm-C, GM-OTA-C & MOSFET-C Filters
- Highly linear continuous-time filters
- Noise and dynamic range
- On-chip tuning techniques
- Conclusions

## GENERAL USES OF CONTINUOUS-TIME FILTERS





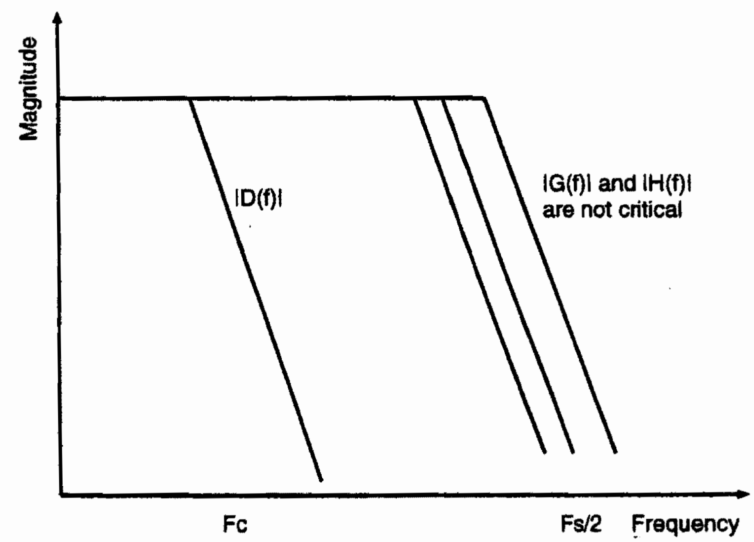

## USE OF CONTINUOUS-TIME FILTER FOR ANTIALIASING/SMOOTHING



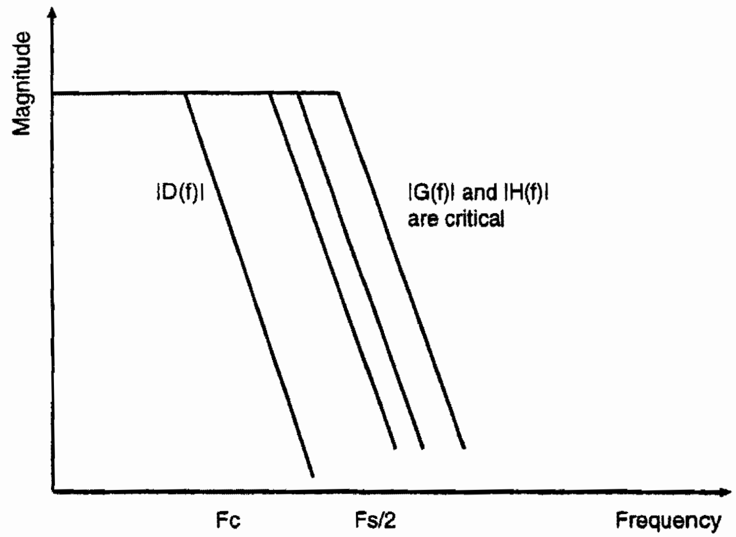

$F_C$ : baseband upper frequency limit

$F_S$ : sampling frequency

(a) If $F_C << F_S/2$:



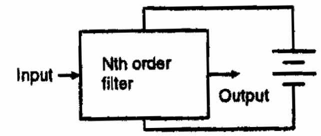
(b) If $F_C$ is close to $F_S/2$:

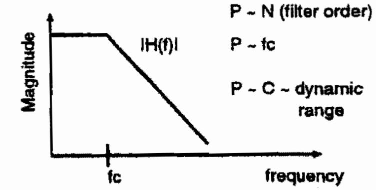


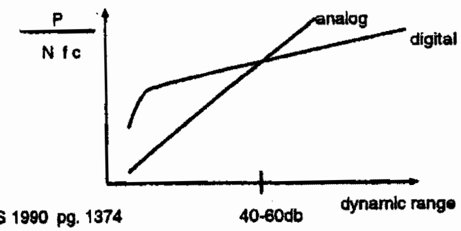

Since H(f) is critical for filter cutoff frequencies and is near fs/2, the continuous-time filter must be well controlled to prevent changes to the passband. Since must control continuous-time filter well, maybe make the entire system continuous-time.



## COMPARISON OF ANALOG AND DIGITAL FILTERS



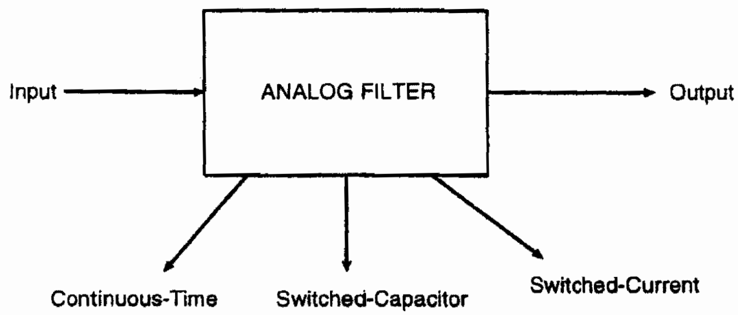




Vittoz, ISCAS 1990 pg. 1374

Issues NOT included in the above comparison

- Advantage of programmability in digital filters
- No manufacturing tolerance of digital filter frequency response
- Overhead of the A/D, D/A, antialiasing and smoothing filter

## CONTINUOUS-TIME AND SAMPLED-DATA FILTERS




- performance of the two is comparable
- switched-capacitor filters do not require a tuning circuit
- continuous-time filters do not suffer from high frequency noise aliasing
- linearity of switched-capacitor circuits generally superior
- most low frequency filters are switched-capacitor in the industry
- Over 10 MHz passbands, continuous-time filter is only choice
- switched capacitors suffer from incomplete settling, switch charge injection, noise aliasing
- continuous-time filters often suffer from tuning circuit feedthrough



## ROUGH ATTRIBUTES OF INTEGRATED CONTINUOUS-TIME FILTERS

- successful for high frequency (up to 100 MHz)
- achieve moderate linearity (e.g. 40-60 dB)
- achieve dynamic range in 60-80 dB range
- frequency response accuracy better than $+-5\%$ with good design
- not presently viable for high-Q, high frequency, high dynamic range applications (eg. A bandpass filter with: Q=100, 10.7 MHz, 100 dB dynamic range)

## STATE-VARIABLE FILTERS

Necessary Building Blocks

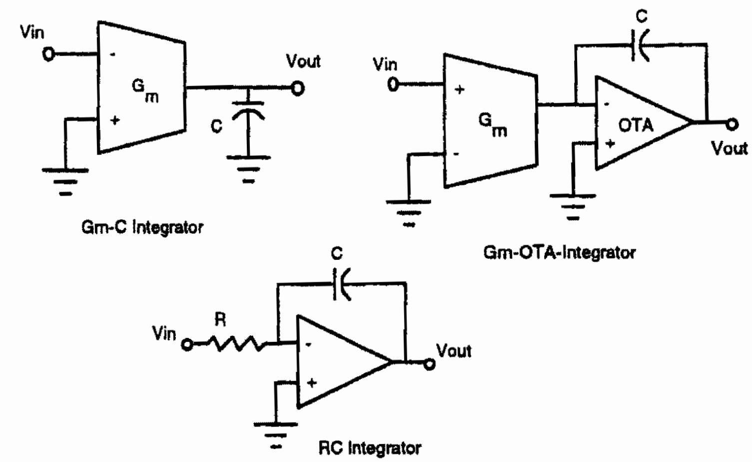
- integrators
- weighted summers

Common Structures

- Cascade of biquads
- Signal flow graph techniques
  - simulation of LC ladder equations (leapfrog filter)



## INTEGRATOR IMPLEMENTATION WITH VARIOUS APPROACHES




For All Integrators

$$\frac{V_o}{V_{in}} = \frac{-\omega_o}{s}$$

$\omega_o = \frac{G_m}{C}$ for Gm-C and Gm-OTA-C integrators.

$\omega_o = \frac{1}{RC}$ for the RC integrator

## STATE VARIABLE SYNTHESIS TECHNIQUES

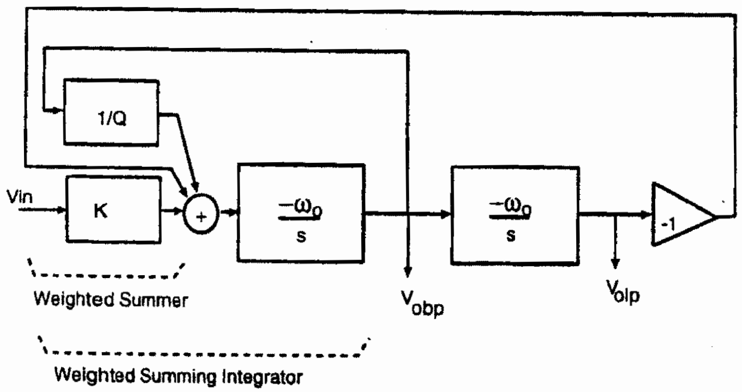
Biquadratic Implementations - The Two Integrator Loop

Second-Order Bandpass Response

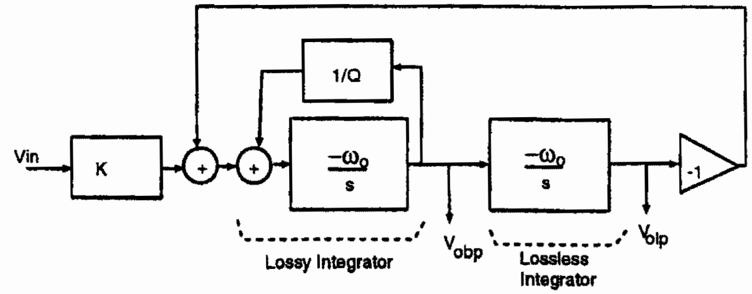
$$V_{obp}(s) = \frac{K\omega_o s}{s^2 + \frac{\omega_o}{Q}s + {\omega_o}^2}V_{in}(s)$$

Second-Order Lowpass Response

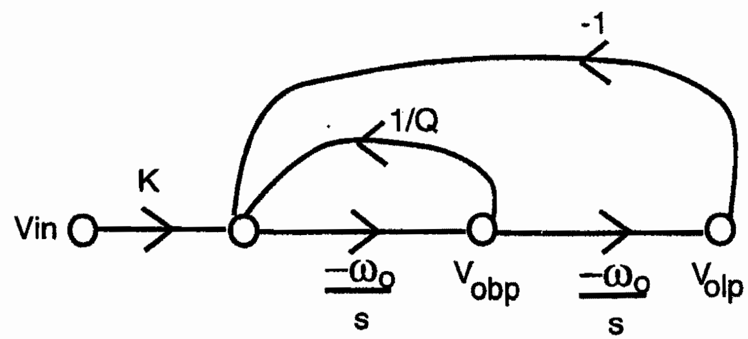
$$V_{olp}(s) = \frac{K{\omega_o}^2}{s^2 + \frac{\omega_o}{Q}s + {\omega_o}^2}V_{in}(s)$$






Equivalent Signal Flow Graph




Generalized Biquadratic Transfer Function

$$V_o(s) = \frac{s^2 + \frac{\omega_{oz}}{Qz}s + {\omega_{oz}}^2}{s^2 + \frac{\omega_{op}}{Qp}s + {\omega_{op}}^2}V_{in}(s)$$

Zero placement in the generalized biquad can be achieved by (i) creating an output signal that is the weighted sum of the two integrator outputs, as well as the input, Vin or (ii) by summing weighted values of the input, Vin, into both integrators.

## ACTIVE LC LADDER SIMULATION

Why LC Ladder Simulation ?

- Wealth of design knowledge exists for passive ladders
- Passband sensitivity is ZERO to component variations (for maximum power transfer design – equal terminations)
- Most cases, lower sensitivity ==> lower noise structure

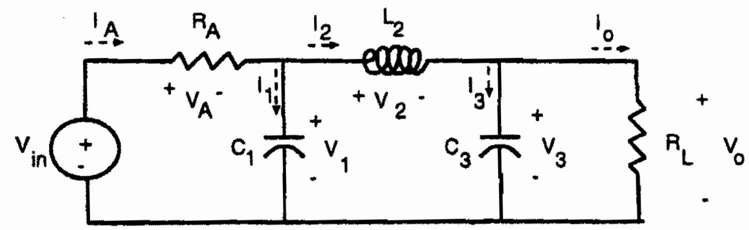
Methods of Ladder Simulation

- operational simulation (e.g. leapfrog filters)
- component by component simulation



## OPERATIONAL SIMULATION OF LC LADDER

**Goal:** Find an active circuit that will simulate every branch voltage and branch current equation of the following passive LC ladder:




Step 1: Write all Branch Equations

$I_A = \frac{V_A}{R_A}, \quad V_1 = \frac{I_1}{sC_1}, \quad I_2 = \frac{V_2}{sL_2} \quad V_3 = \frac{I_3}{sC_3} \quad I_O = \frac{V_O}{R_L}$

$V_A = V_{in} - V_1 \quad V_2 = V_1 - V_3, \quad V_O = V_3 \quad I_1 = I_A - I_2$

$I_3 = I_2 - I_O$

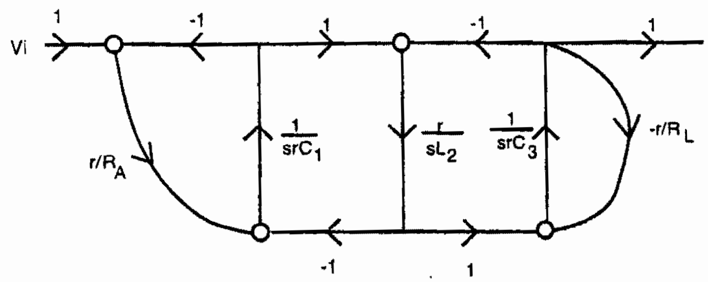
Step 2: Scale all Currents by r

All currents are scaled by an arbitrary resistance (e.g. $r = 1\Omega$) so that the input/output relations of the integrators are dimensionless. $rI_A = \frac{rV_A}{R_A}, \quad V_1 = \frac{rI_1}{srC_1}, \quad rI_2 = \frac{V_2}{sL_2/r} \quad V_3 = \frac{rI_3}{srC_3}$

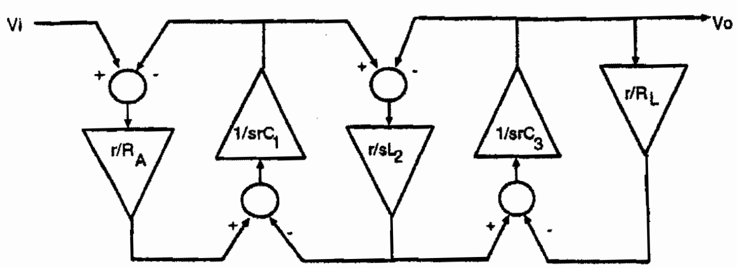
$rI_O = \frac{rV_O}{R_L} \quad V_A = V_{in} - V_1 \quad V_2 = V_1 - V_3, \quad V_O = V_3$

$rI_1 = rI_A - rI_2 \quad rI_3 = rI_2 - rI_O$

## Resulting Active Filter

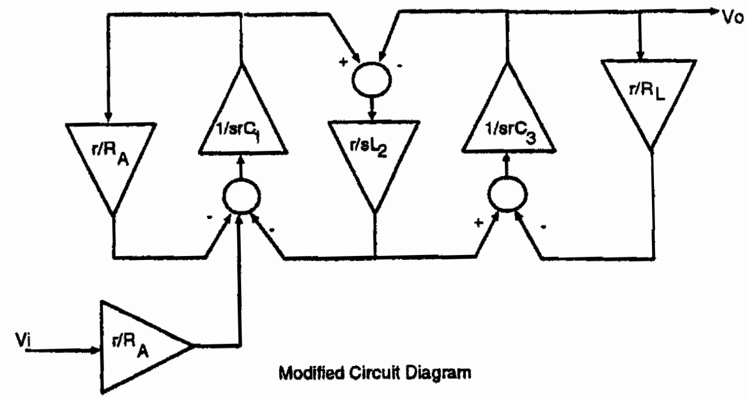



Signal Flow Graph Format

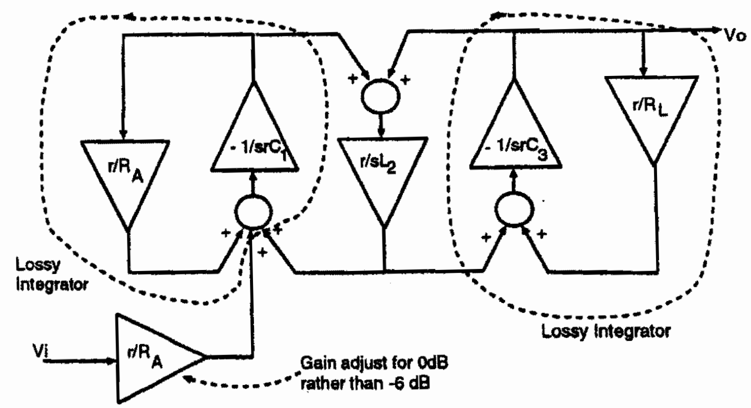



Circuit Block Diagram



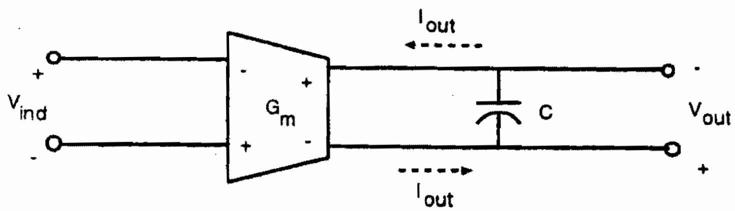



Modified Circuit Diagram




Final Block Diagram

## TRANSCONDUCTOR-C FILTERS




$$H(s) = \frac{G_m}{sC} = \frac{\omega_o}{s}$$

Ideal Integrator

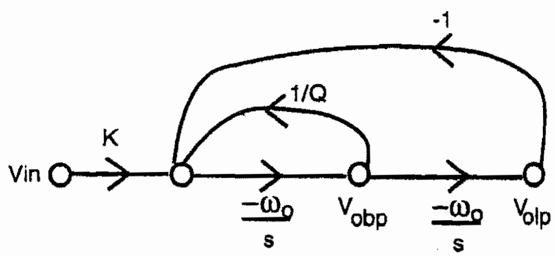
- infinite gain at DC
- unity gain at $\omega_o$
- phase shift of $-\pi/2$ radians for all frequencies



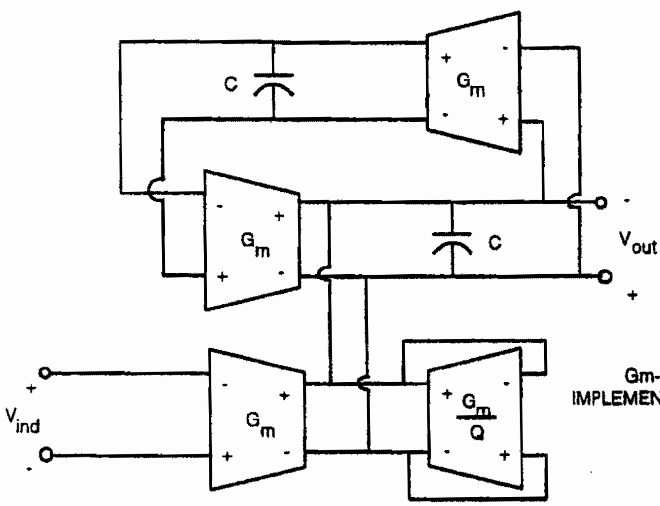
## CHARACTERISTICS OF A GOOD TRANSCONDUCTOR

- high input impedance
- high output impedance
- large signal handling capability at the input and output terminals (with low distortion)
- high DC gain
- wide bandwidth
- well defined and tunable V$-$ >I mechanism

## IMPLEMENTATION OF A STATE-VARIABLE BIQUAD




SIGNAL FLOW GRAPH

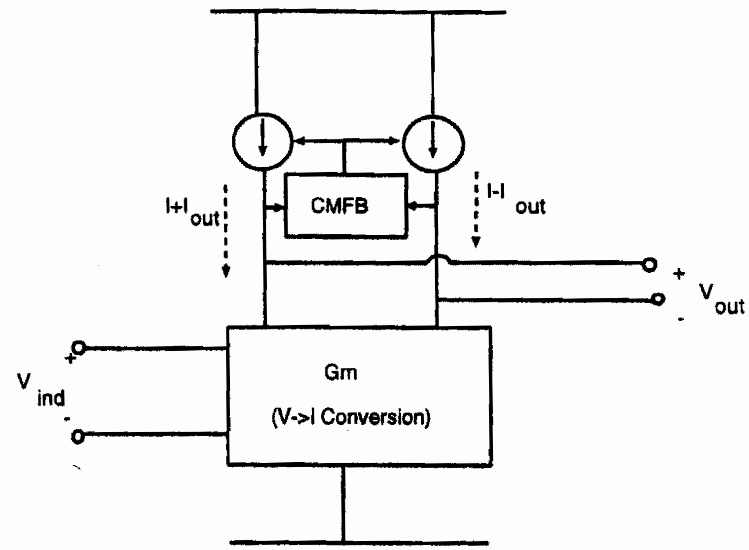



Gm-C IMPLEMENTATION

- signal summation achieved by paralleling transconductor outputs
- Damping provided by an equivalent resistance of value $Q/G_m$.



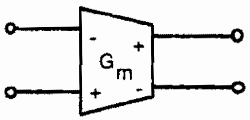
## TRANSCONDUCTOR DESIGN APPROACHES



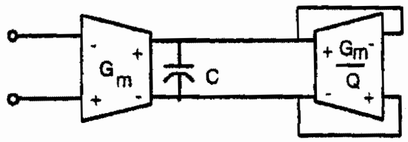

Two Primary Design Issues

- V − > I conversion
- Obtaining high output conductance

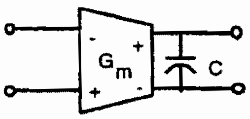
## SUMMARY OF TRANSCONDUCTOR BUILDING BLOCKS



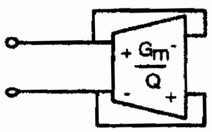

Transconductor



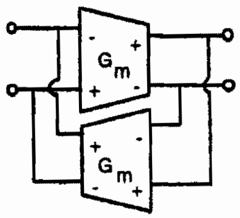

Lossy Integrator




Lossless Integrator



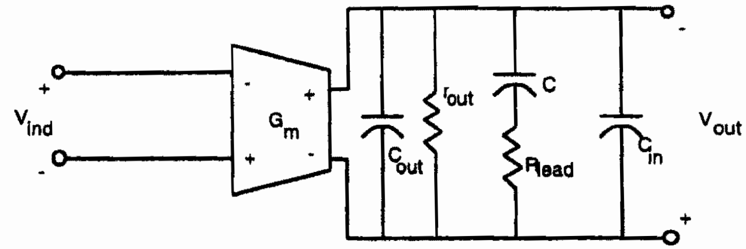

Resistor




Gyrator



## TRANSCONDUCTOR-C INTEGRATOR PHASE ERRORS

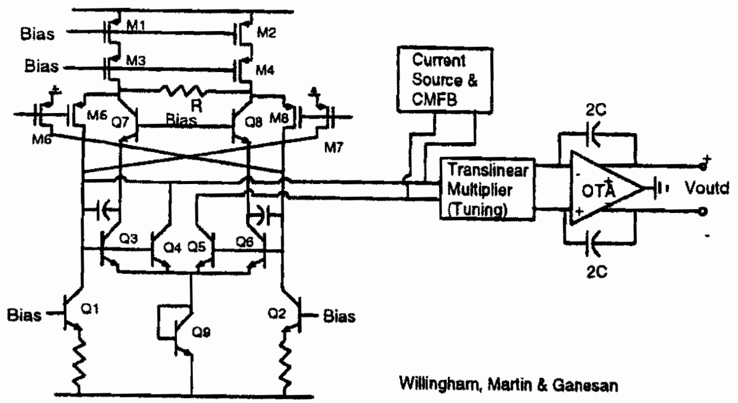



$$H_a(s) = \frac{G_{mo}(1 + s/\omega_z)}{(1 + s/\omega_p)} \frac{r_{out}}{1 + s r_{out}(C + c_{out} + c_{in})}$$

$$\phi_{I-error} \approx \pi/2 + (\omega/\omega_z) - (\omega/\omega_p) - arctan[A_o(\omega/\omega_{ox})]$$

- 20 MHz $G_m - C$ Bessel filter
- $C = 1pF, G_{mo} = 125.7\ \mu S$
- $r_{out} \approx 1M\Omega$
- ==> $A_o = 126$ ( low DC gain introduces phase lead at low freq)
- transconductor parasitic pole at 300 MHz (no zero)
- phase error at 20 MHz: $-3.4^o$
- modest phase lead can be added with resistor in series with load capacitor to create a high frequency zero
- high Q requires phase control servo loop

## A HIGHLY LINEAR BICMOS GM-OTA-C INTEGRATOR




- basic transconductance set by resistance, R
- negative feedback used to reduce source follower impedance (M5, M8)
- feedback loop: M5, Q1, Q3 and Q7
- feedback loop: M8, Q2, Q6 and Q8
- Gm output mirrored from Q3,Q6 to Q4, Q5.
- tuning circuit does not impact signal swing
- OTA increases gain, splits poles and prevents loading



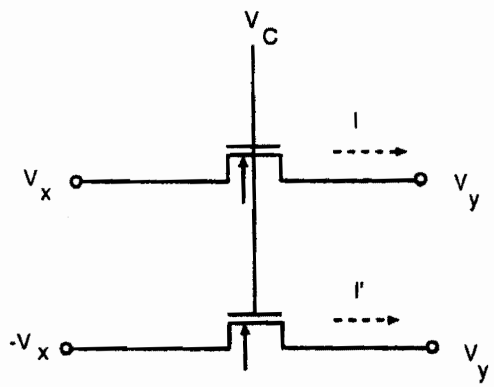
## MOSFET-C FILTERS

Basic Concept

- similar to Gm-OTA-C Implementation
- except replace Gm with a passive element (e.g. resistor) as opposed to one that dissipates power
- instead of using resistors, use MOSFETs in triode region
- fully balanced design will eliminate even-order nonlinearities
- depending on application and load driving needs, may require an OPAMP or an OTA

# NONLINEARITY CANCELLATION IN BALANCED MOSFETS

Consider two matched MOSFETS




$$(1)\quad I = G(V_C)(V_x - V_y) + a_2[(+V_x)^2 - V^2{}_y]$$

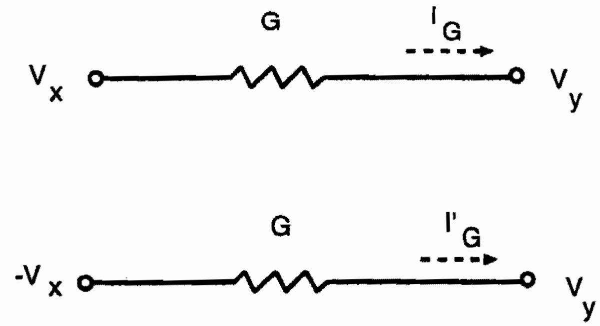
$$(2)\quad I' = G(V_C)(-V_x - V_y) + a_2[(-V_x)^2 - V^2{}_y]$$

$$(1)-(2)\quad I - I' = 2G(V_C)V_x$$

$$G(V_C) = \frac{W}{L}\mu C'_{ox}(V_C - V_T)$$

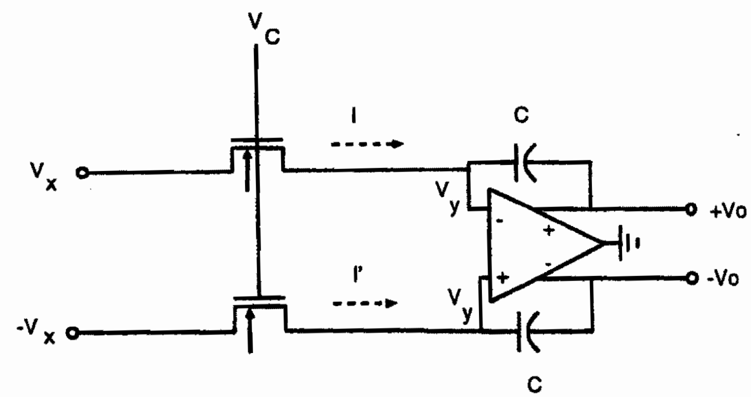


## Compare with two Linear Resistors




$$I_G - I'_G = 2GV_x$$

## The Fully Balanced MOSFET-C Integrator



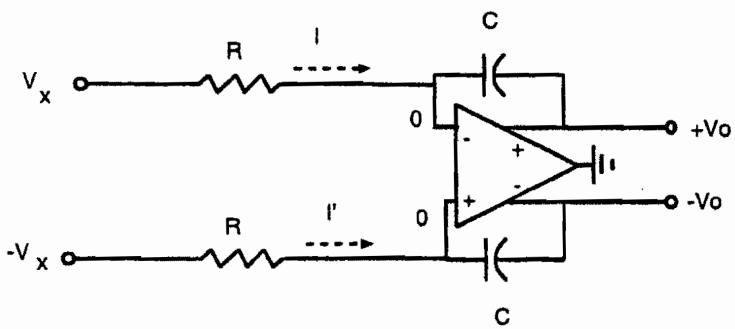

$$(1)\quad V_o(t) = V_y(t) - \frac{1}{C}\int_{-\infty}^{t} I(\tau)d\tau$$

$$(2)\quad -V_o(t) = V_y(t) - \frac{1}{C}\int_{-\infty}^{t} I'(\tau)d\tau$$

$$(1) - (2)\ \ V_o(t) - -V_o(t) = \frac{-1}{C}\int_{-\infty}^{t}[I(\tau) - I'(\tau)]\, d\tau$$

$$V_o(t) = \frac{-1}{RC}\int_{-\infty}^{t} V_x(\tau)d\tau$$

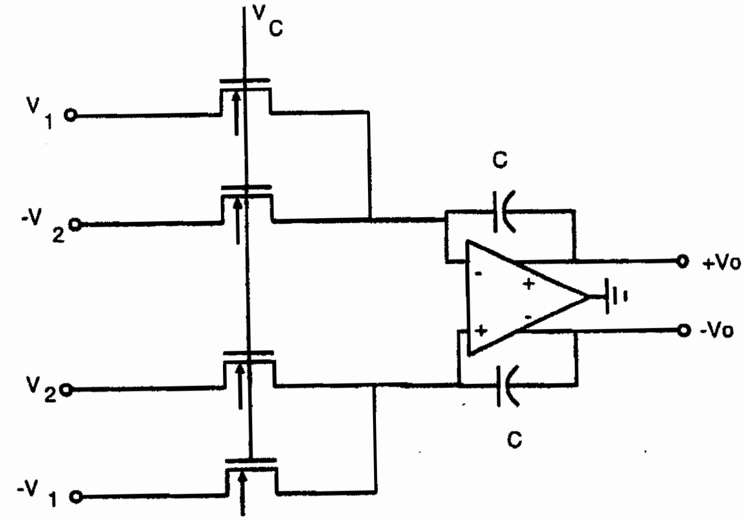
Consider a Fully Balanced RC Integrator




The input/output relationship is identical to the MOSFET-C integrator; however, internally the circuits differ. The RC integrator is linear so the virtual ground inputs of the opamp stay at 0 V, but $V_y$ differs from zero. In fact, $V_y$ follows the second order nonlinearity of the MOS transistors.

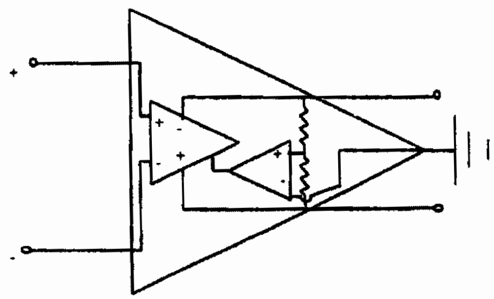


Differential Balanced Integrator - Balanced and Linear

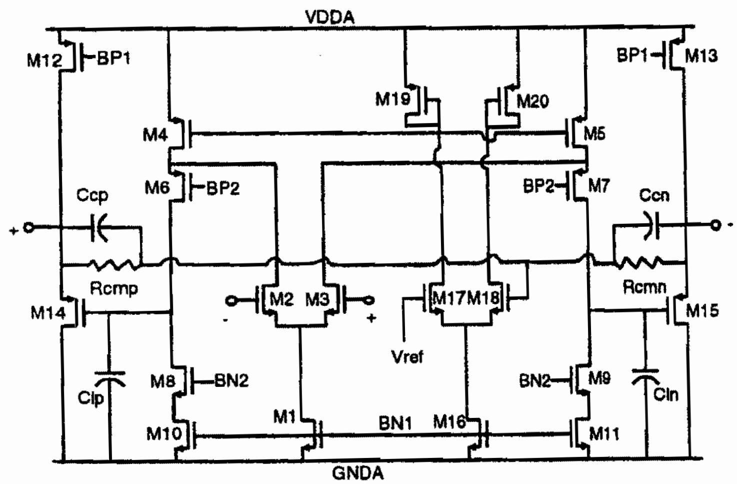



Balanced structure is immune to common-mode noise such as substrate coupling.

## BALANCED OPAMP DESIGN STYLE



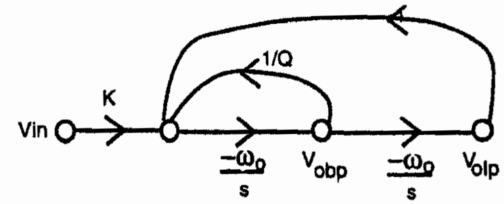

## A Fully Balanced Folded-Cascode Opamp



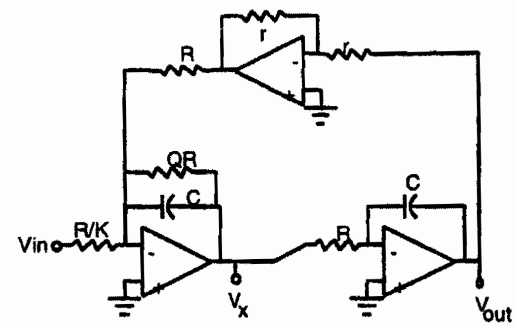



## MOSFET-C TOW-THOMAS BIQUAD

### Signal Flow Graph & Active RC Tow-Thomas Biquad

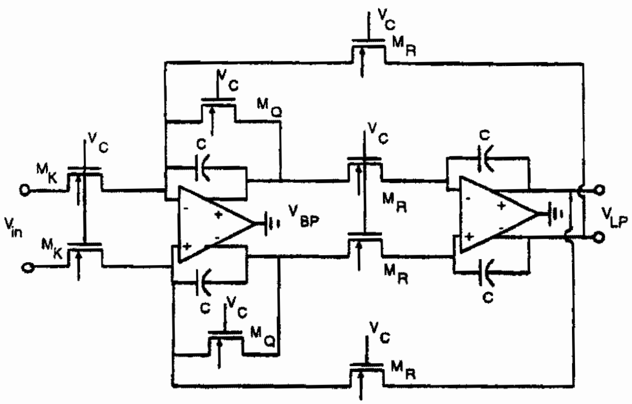



SIGNAL FLOW GRAPH



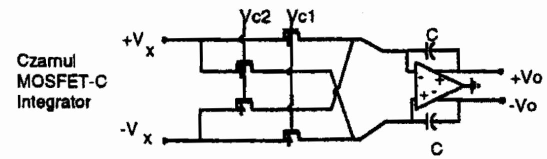

TOW-THOMAS BIQUAD IMPLEMENTATION

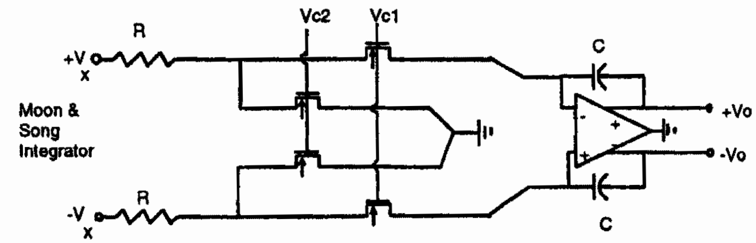
## MOSFET-C Equivalent of Tow-Thomas Biquad






## HIGHLY LINEAR R-MOSFET-C FILTERS

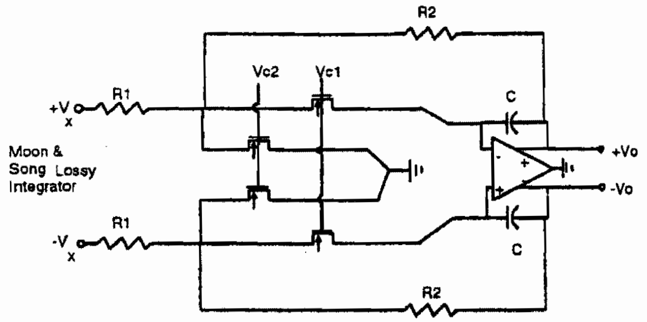



Attributes: Lossless Integrator

- Voltage drop occurs primarily across resistor ==> small MOSFET $V_{DS}$ ==> excellent linearity
- linearity to 90 dB
- generally low frequency applications (digital audio)

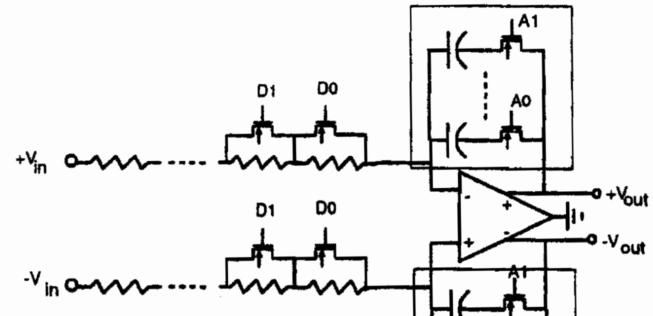
## Lossy Integrator




- negative feedback improves linearity further
- loss of loop gain ==> reduced frequency of operation



## PROGRAMMABLE ACTIVE RC FILTERS




MOS devices used as switches

Durham,Hughes & Redman-White
(also Khorramabadi,Tarsia &Woo)
(also Shariatdoust,Nagaraj,Khoury, et-al)

- program capacitors, resistors or both to frequency tune filter
- excellent for high dynamic range applications
- excellent linearity (independent of matching to first order)
- programming achieved with digital counters and/or DSP ==> no tuning circuit feedthrough
- tuning resolution limited
- infinite hold time for tuning circuit
- switch parasitic capacitance and series resistance can alter frequency response
- bandwidth achievable slightly less than MOSFET-C filter approach

## Maximizing Dynamic Range

- large capacitor ==> low R (or high Gm) ==> large power dissipation & difficult to drive impedances
- large capacitor ==> large chip area
- high signal swing ==> high vdd
- high signal swing ==> better linearization methods required
- high signal swing difficult with filter offsets
- high temperature ==> higher noise



## ON-CHIP TUNING TECHNIQUES

Two Primary Items To Be Tuned

- Frequency scaling (i.e. time constant control )
- Q control (i.e. phase shift adjustment in critical feedback loops)
- For integrator: frequency scaling => unity-gain frequency control and Q-control => phase shift adjustment

Two Basic Approaches to Tuning

- Indirect tuning or "Master-slave" tuning
- Direct tuning for extremely accurate response (e.g. necessary for very high-Q filters)

# MASTER-SLAVE FREQUENCY TUNING: Reference Resistor

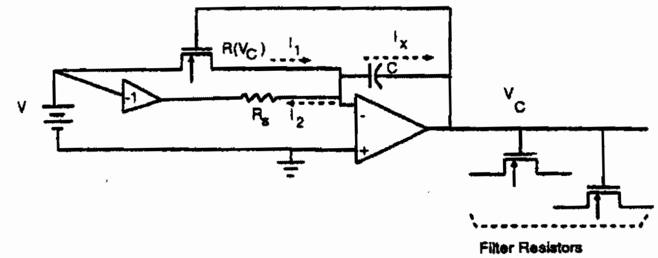
## Basic Idea

RC products of filter are accurately controlled by two steps:

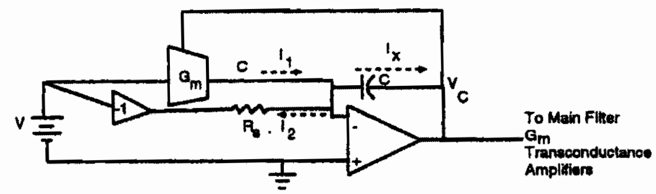
1. At manufacture, trimming is performed at test time to remove the effect of capacitor errors due to processing. (This can be done by adjusting R or C)
2. In operation, a precision off-chip resistor serves as a reference that the internal resistors or $G_m$ stages track with a feedback control loop.
3. Accuracy depends on matching of tuning circuit resistor to main filter (slave)



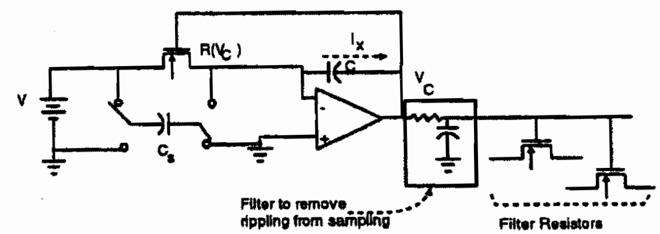
## Reference Resistor Tuning Circuit




Circuit Stabilizes when Ix=0. V should be small to avoid transistor nonlinearities
(Fully Differential Approach could be used to avoid the small V requirement)




## Reference Switched-Capacitor Resistor Tuning Circuit

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## COURSE CONCLUSION

- The following material was described:
  - Overview of applications for continuous-time filters
  - Fundamentals of popular continuous-time filter techniques
  - State-variable synthesis techniques
  - Gm-C, GM-OTA-C and MOSFET-C filters
  - Noise and dynamic range
  - On-chip tuning techniques
- The field of continuous-time filters is continually evolving
- Research directions focused on linearity improvement techniques and low power supply voltage operation
- Continuous-time filters are excellent in moderate dynamic range applications but need considerable improvement before usable in high Q high dynamic range applications.



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